WHAT IS CLAIMED IS:

1. A system for recovering and aligning synchronous data transmissions, comprising:

a transmitter configured to transmit a source clock signal and a plurality of data groups over a plurality of channels, the plurality of data groups being transmitted during the same clock cycle pursuant to the source clock signal, each data group being transmitted over a corresponding channel; and

a receiver configured to receive the source clock signal and the plurality of data groups over the plurality of channels, the receiver further configured to include:

for each channel: (a) a local clock configured to generate a local clock signal based on the source clock signal, the local clock signal being phase-shifted from the source clock signal by a predetermined amount of phase shift, (b) a logic device configured to clock in the data group received over the channel using the local clock signal, (c) a sequence number generator configured to generate a sequence number associated with the data group, (d) a FIFO buffer configured to store and output the clocked-in data group and the associated sequence number, (e) a memory device configured to store the clocked-in data group from the FIFO buffer using the associated sequence number as a memory address, the memory device further configured to output a predetermined portion of its contents after a predetermined capacity threshold is reached.

2. The system of claim 1 wherein the transmitter is further configured to transmit a start-of-cell signal to the receiver; and

wherein upon the receiver detecting the start-of-cell signal having a specific value for a predetermined cycle period, the sequence number generators are synchronized.

3. The system of claim 1 wherein the receiver is implemented using a plurality of field programmable gate arrays.

4. The system of claim 3 wherein the local clock is implemented using a digital clock manager associated with a field programmable gate array.

5. The system of claim 1 wherein the predetermined amount of phase shift is determined empirically.

6. The system of claim 1 wherein the predetermined amount of phase shift is calculated based on respective latency delays of the source clock signal and a corresponding channel.

7. The system of claim 1 wherein each data group includes a plurality of data signals; and

wherein the plurality of data signals within each data group have the same latency delay over the corresponding channel.

8. The system of claim 1 wherein the memory device is a dual port random access memory.

9. The system of claim 1 wherein the sequence number generator is incremented every clock cycle pursuant to the local clock signal.

10. A backplane incorporating the system as recited in claim 1.

11. A system for recovering and aligning synchronous data transmissions, comprising:

a transmitter configured to transmit a source clock signal and a plurality of data groups of over a plurality of channels, wherein a set of data groups collectively forming a data word is transmitted during each clock cycle pursuant to the source clock signal, each data group in the set of data groups being transmitted over a corresponding channel; and

a receiver configured to receive the source clock signal and sets of data groups over corresponding channels, the receiver including:

a plurality of local clocks, each local clock configured to generate a local clock signal based on the source clock signal, the local clock signal being phase-shifted from the source clock signal by a predetermined amount of phase shift;

a plurality of devices, each device configured to receive and clock in corresponding data groups from a corresponding channel using the local clock signal from a corresponding local clock;

a plurality of sequence number counters, each sequence number counter associated with a corresponding device and configured to provide respective sequence numbers for data groups received by the corresponding device;

a plurality of buffers, each buffer configured to store and output clocked-in data groups from a corresponding device and their associated sequence numbers; and

a plurality of memory devices, each memory device configured to store the clocked-in data groups from a corresponding buffer using their associated sequence numbers as memory addresses, each memory device further configured to output a predetermined portion of its contents after a predetermined capacity threshold is reached.

12. The system of claim 11 wherein the transmitter is further configured to transmit a start-of-cell signal to the receiver; and

wherein upon the receiver detecting the start-of-cell signal having a specific value for a predetermined cycle period, the sequence number counters are synchronized.

13. The system of claim 11 wherein the receiver is implemented using a plurality of field programmable gate arrays.

14. The system of claim 13 wherein the local clocks are implemented using two or more digital clock managers associated with plurality of field programmable gate arrays.

15. The system of claim 11 wherein the predetermined amount of phase shift associated with each local clock is determined empirically.

16. The system of claim 11 wherein the predetermined amount of phase shift associated with each local clock is calculated based on respective latency delays of the source clock signal and a corresponding channel.

17. The system of claim 11 wherein each data group includes a plurality of data signals; and

wherein the plurality of data signals within each group have the same latency delay over the corresponding channel.

18. The system of claim 11 wherein the plurality of memory devices include a dual port random access memory.

19. The system of claim 11 wherein each sequence number generator is incremented every clock cycle pursuant to the local clock signal associated with a corresponding local clock.

20. A backplane incorporating the system as recited in claim 11.

21. A method for recovering and aligning synchronous data transmissions, comprising:

transmitting a source clock signal and a plurality of data groups from a transmitter to a receiver per clock cycle pursuant to the source clock signal, the plurality of data groups collectively forming a data word;

at the receiver:

using the source clock signal to create a plurality of local clock signals, each local clock signal being phase-shifted from the source clock signal by a corresponding predetermined amount of phase shift;

clocking in each data group using a corresponding local clock signal;

assigning a sequence number to each clocked-in data group;

storing each clocked-in data group and its assigned sequence number in a corresponding buffer;

reading out each clocked-in data group and its assigned sequence number from its corresponding buffer; and

storing each read-out data group into a corresponding dual port memory using the assigned sequence as its memory address.

22. The method of claim 21 further comprising:

sending a special start-of-cell signal and an alignment cell from the transmitter to the receiver;

at the receiver, upon detecting the special start-of-cell signal, initializing sequence numbers to be assigned to clocked-in data groups to a starting value, the starting value being embedded in the alignment cell.

23. The method of claim 21 further comprising:

at the receiver, incrementing the sequence number for future assignment to a next clocked-in data group.

24. The method of claim 21 further comprising:

at the receiver, reading out a predetermined portion of each dual port memory.

25. The method of claim 21 wherein the corresponding predetermined amount of phase shift for each local clock signal depends on the respective latency delays of the source clock signal and a corresponding data group.

26. A backplane utilizing the method as recited in claim 21.